TELEPRINTER INPUT/OUTPUT TO A SMALL COMPUTER

A Thesis Submitted
in partial fulfilment of the requirements

for the degree of
MASTER OF TECHNOLOGY

by
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to the
Department of Electrical Engineering
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KANPUR

1968

This is to certify that this work on TELEPRINTER INPUT/OUTPUT to a SMALL COMPUTER has been carried out under my supervision and it has not been submitted elsewhere for a degree.

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August 1968

ACKNOWLEDGEMENT

The author wishes to express his appreciation to Dr. H.N. Mahabala for suggesting the problem, for his guidance and advice and for directing this work.

The author also wishes to thank Dr V. Rajaraman, Dr. T.R. Viswanathan and Professor D.L. Stephenson for their valuable suggestions.

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August 1968

SYNOPSIS

A complete system design for interfacing a Teleprinter Unit to a small digital computer is discussed in detail. The system has been tested out using DEC Modules and will be implemented using modules developed at Indian Institute of Technology, Kanpur.

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CHAPTER I

INTRODUCTION

The input-output device provides a means of communication between the computer and the outside world. A wide variety of devices is available for this purpose. The choice of the device to be used depends primarily on the application to which the system is to be put. A Teleprinter unit is quite suitable for use with a small digital computer. There is also the possibility of using it as a remote unit to a larger system at a later stage. In order to use indigenously made components and devices to the extent possible, it was decided to use the Hindustan Teleprinter Unit Model T2-CN.

A Teleprinter is essentially a serial device. Furthermore, due to the presence of electromechanical components, it is also a slow device compared to the speed of the electronic circuits used in the system. These characteristics impose certain constraints on the design of the interface system. The disadvantages of a slow speed input/output can be partially offset by overlapped operation, i.e. when the input/output unit is busy, the CPU can perform other functions within the computer.

Serial-to-parallel conversion (and vice versa) will be necessary and can be accomplished by use of buffer registers. Buffers are

temporary storage locations into which information from one medium can be read-in at one speed and then read-out at a different rate. Parallel transfer of information is also possible in these registers.

One additional problem involved in the process is that of code conversion. The standard Teleprinter code is not suitable for use in computers where the digits 0 through 9 are coded in their straight binary order. This would normally involve the use of a matrix array of diodes/transistors. An economical solution to the problem can be obtained by inverting and/or transposing the information pulses. For this purpose, the Key Board pattern and hence the Type Bar settings on the Teleprinter unit have to be modified. As a result, only a simple logic is required to convert a portion of one code group to another.

Two modes of operation of the unit are needed - BCD and OCTAL. In BCD mode, a word in computer memory would be composed of two, six-bit characters; whereas in OCTAL mode, there are four, three-bit octal digits to a word.

One other feature necessary is the ERASE facility. It is always possible to mistype a character while keying-in the information. In such a case, by pressing the ERASE button (on the console) the whole word is cleared and the operator can now re-enter the word.

CHAPTER II

THE TELEPRINTER

Main Features

The input-output device to be used in connection with the small digital computer is the standard Hindustan Teleprinter, Model T2-CN (Page, Automatic, Send-Receive type). Typing-in of information is limited by the speed of the operator while the printing-out of information is done at a rate of upto 400 characters per minute. The teleprinter can also read-in or punch-out perforated paper tape at a rate of 400 characters per minute. Signals transferred between the teleprinter and the control logic are the standard, serial, 7.5 unit code. The signals consist of SPACES and MARKS, which correspond to POSITIVE and NEGATIVE bias currents in the teleprinter and to logical ONES and ZEROS in the control and the computer. The START space and the subsequent five information bits are one unit of time duration each (one unit of time being equal to 20 m sec) and are followed by a STOP mark of one and half units of time duration. Thus it takes a total of 150 m sec to transmit one character, as illustrated in figure 2.1 for a typical character, say A.

The five bit code used by the Teleprinter is the standard CCITT, five-unit, No. 2 code. With five bits, we can code 32 characters, each of which may represent a letter or a figure. This

makes for a total of 64 combinations. Twenty six of these have been chosen to represent two alphanumeric characters each : a letter and a figure. Two special shift characters, LETTERS and FIGURES, whose effect remain until changed, serve to discriminate between the two characters of the same code. The standard code set is illustrated in Appendix B.

Other Features

1. Motor: The teleprinter is driven by a commutator-type motor.
2. Two colour printing: To provide an easy means of distinguishing between the out-going and the incoming messages, the Teleprinter prints the former in RED and the latter in BLACK.
3. Runout key: The printer is fitted with a Run-out key which uninterruptedly sends the combination corresponding to the last key pressed down by the operator.

Because of code-conversion problems, certain modifications were introduced on the Key Board of the Teleprinter Unit. These details are discussed in the following chapter.

CHAPTER III

MODIFICATIONS TO THE EXISTING TELEPRINTER

The standard coding of characters in the Teleprinter is not suitable for use in a digital computer. In the computer, numerals 0 through 9 are coded in their straight binary order. This involves the use of code conversion matrices. However, we simplify the problem by a slight modification of the bit pattern so that the digits 0 through 9 are obtained in their straight binary order directly from the Teleprinter. This necessitates a modification of the Key Board pattern and the Type Bar Settings. These modifications, alongwith the modified codes, are shown in the Appendix C.

With five bits, we can have 32 combinations; of these, only 26 are used for alphanumeric information. By inspection of the standard code set we find that the normal binary codes corresponding to digits 0 and 4 are not included in this set of 26. Hence we need to modify the bit pattern to ensure that the straight binary configurations for all digits 0 to 9 will come within this set. A digital computer program was written to find the minimal key board pattern allowing for inversion and/or transposition of signal bits.

Consider the bit pattern for the characters Y (letter shift)/ 6 (figure shift):

0 1 0 1 0

Here we observe that by complementing bits two and four, this code can very well represent the digit zero. This inversion should, of course, be consistent for all characters (in the same relative positions also); furthermore, digits 0 through 9 should be included in this set. In fact the program written for this purpose tried out all possible combinations of bit patterns (normal and complemented - like for instance, one case may be with bit 1 inverted, another may be with bits 2 and 3 inverted and so on) and came up with four possible alternatives (Refer: Appendix D). Out of these, set 3 was selected as it involved a minimum number of inversions (bits two and four only). Thus what was originally the code for number six would now be the code for number zero. In order to ease typing in the new code, this will mean replacing the key for digit six with that for digit zero. If we did not attempt to do this, the operator will have to use a chart depicting the relation between the original key board set and the corresponding character set after modifications. This monotony on the part of the programmer is avoided by simply inter-changing the relevant keys on the Key Board and also modifying the Type Bar settings accordingly. These charts, of the original and the modified settings, are illustrated in Appendices C1 and C2. With the new Key Board arrangement, the code set by the Teleprinter for the character keyed-in is directly entered into the shift register, of course, after complementing the second and the fourth bits. This way we have

now solved (or, in fact, avoided) the problem of elaborate code-conversion matrices. What we need is only a simple logic to complement the necessary bits.

CHAPTER IV

INPUT/OUTPUT CONTROL UNIT

An overall functional block diagram of the input/output unit and its interaction with the rest of the computer is shown in figure 4.1. Here we observe that both Reading-In and Printing-Out of information are under program control. For each word to be read-in (printed-out) the CPU sends over to the input/output control unit a READ (WRITE) pulse and a mode selecting signal (BCD or OCTAL). These information act on the input/output control logic and depending on the mode selected, either two or four characters are Read-In (Printed-Out). At the end of this operation the input/output control unit sends out an OP COMPLETE signal which is converted into a level (by resetting a flip flop) and then transmitted on to the CPU. Since it takes a fairly long time to read-in (print-out) information from the Teleprinter, the CPU can perform other functions during the period and at specific instants, it can interrogate the OPCOMPLETE line to see whether the input/output is complete or not. The OPCOMPLETE line is normally down (in the logical ONE state) when neither reading-in nor printing-out. However, as soon as either of these operations begin, the line goes up (to the logical ZERO state) signifying that the input/output unit is busy and continues to stay

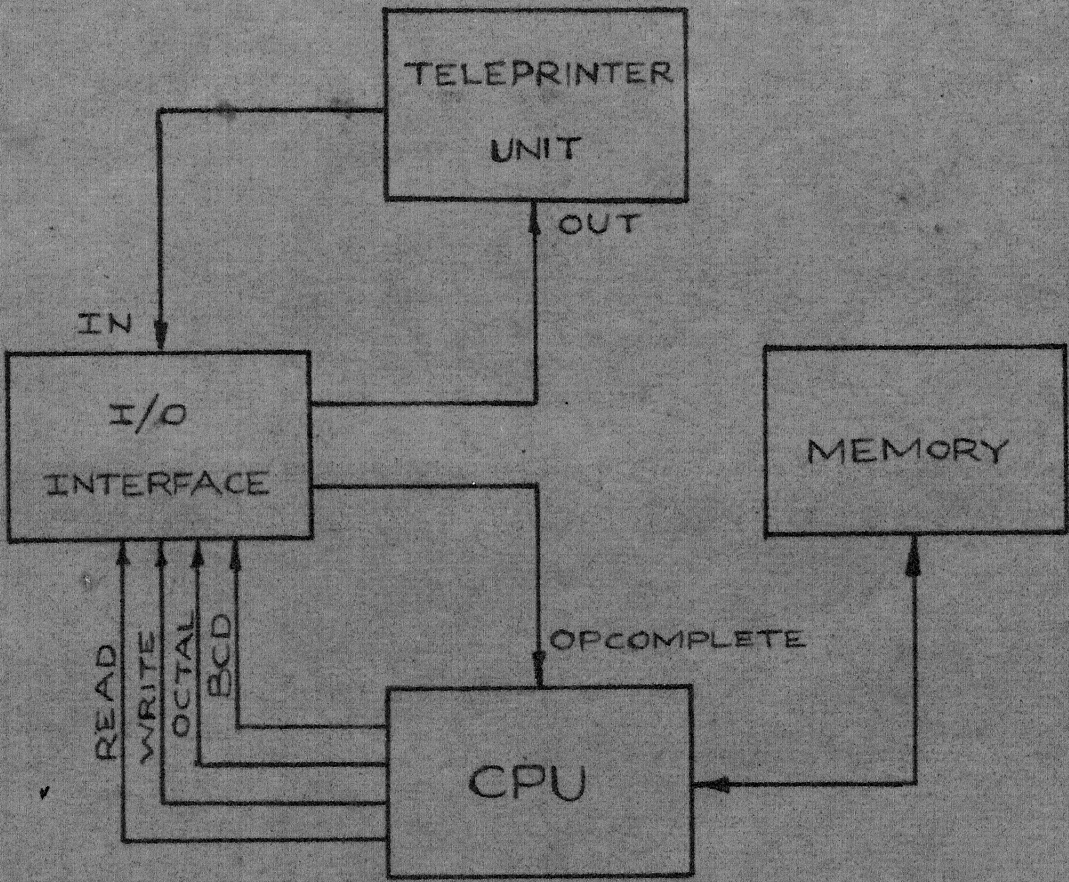


FIG 4.1: OVERALL BLOCK DIAGRAM OF THE I/O UNIT IN RELATION TO THE REST OF THE COMPUTER

in that state till the input/output is complete.

A complete logic of the input/output and its control is shown in figure 4.2. In the following chapters, the Input and Output systems are discussed seperately.

CHAPTER V

INPUT TO THE COMPUTER

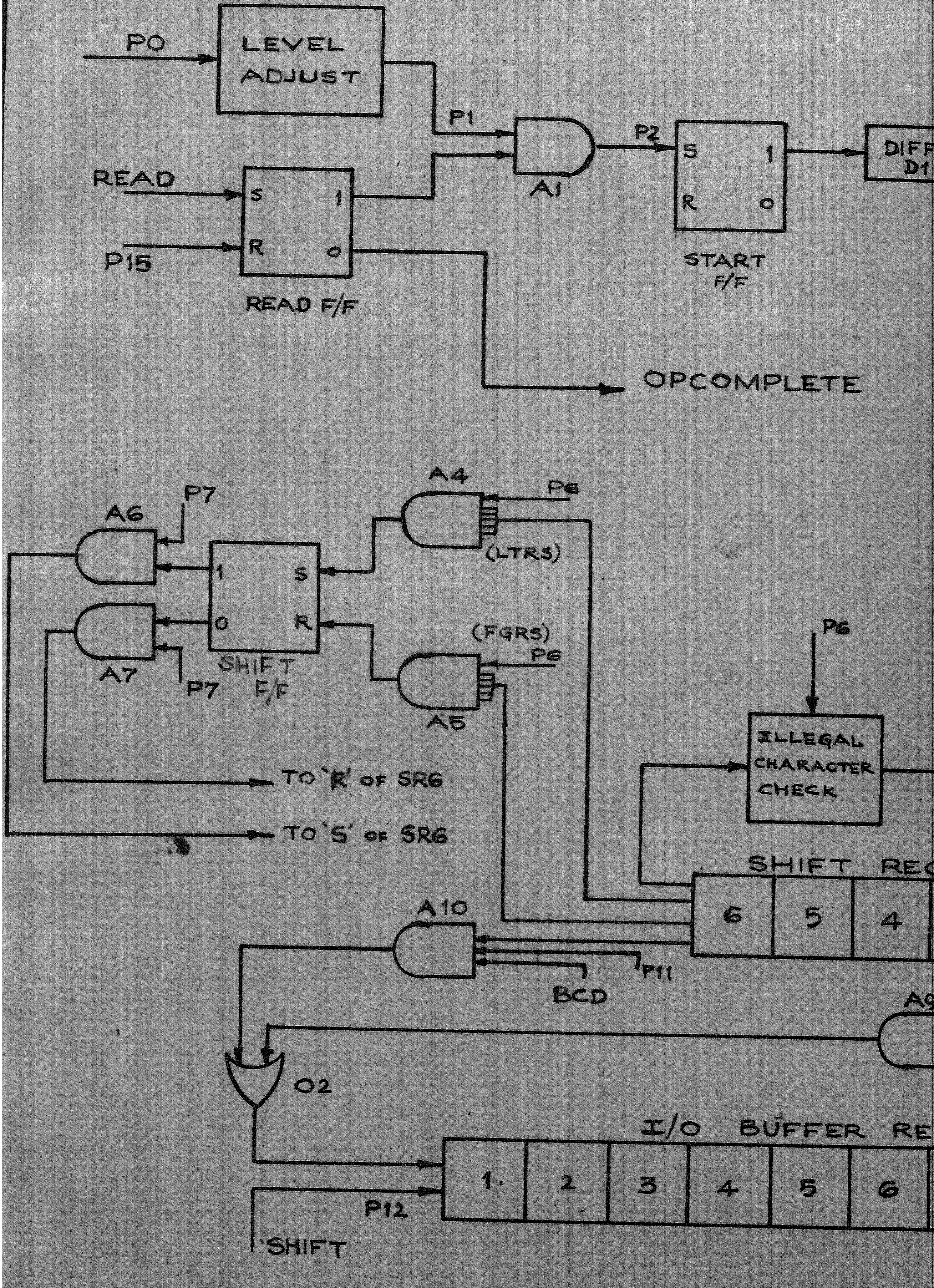
The two basic problems in interfacing a Teleprinter Unit to a computer are:

1. Serial-to-parallel conversion; and
2. Code translation

The problem of code translation has been considerably simplified in our case by rearrangement of keys on the Teleprinter Key Board (Chapter III). Serial-to-parallel conversion is achieved by assembling the serial information into a shift register. Preliminary processing of information is done at this stage after which the information is transferred to the Input/Output Buffer Register.

The complete logic diagram of the Input to the computer and its associated timing diagram are shown in figures 5.1A and 5.1B.

Upon receipt of a READ command from the CPU, the READ flip flop is set thus enabling gate A1 to transmit information from the Teleprinter to the computer. Simultaneously, the OPCOMPLETE line goes up (to the logical ZERO state) thus indicating to the CPU that the input unit is busy. The unit is now ready to read a word, composed of either two (BCD) or four (OCTAL) characters, into the computer memory.



PO
LEVEL ADJUST
P1
P2
A1
READ
P15
READ F/F
START F/F
DIFF D1
OPCOMPLETE
A4
P6
(LTRS)
A6
P7
SHIFT F/F
A7
(FGRS)
A5
TO 'R' OF SR6
TO 'S' OF SR6
ILLEGAL CHARACTER CHECK
SHIFT REG
6
5
4
A10
P11
BCD
O2
I/O BUFFER RE
1.
2
3
4
5
6
P12
SHIFT

FIG

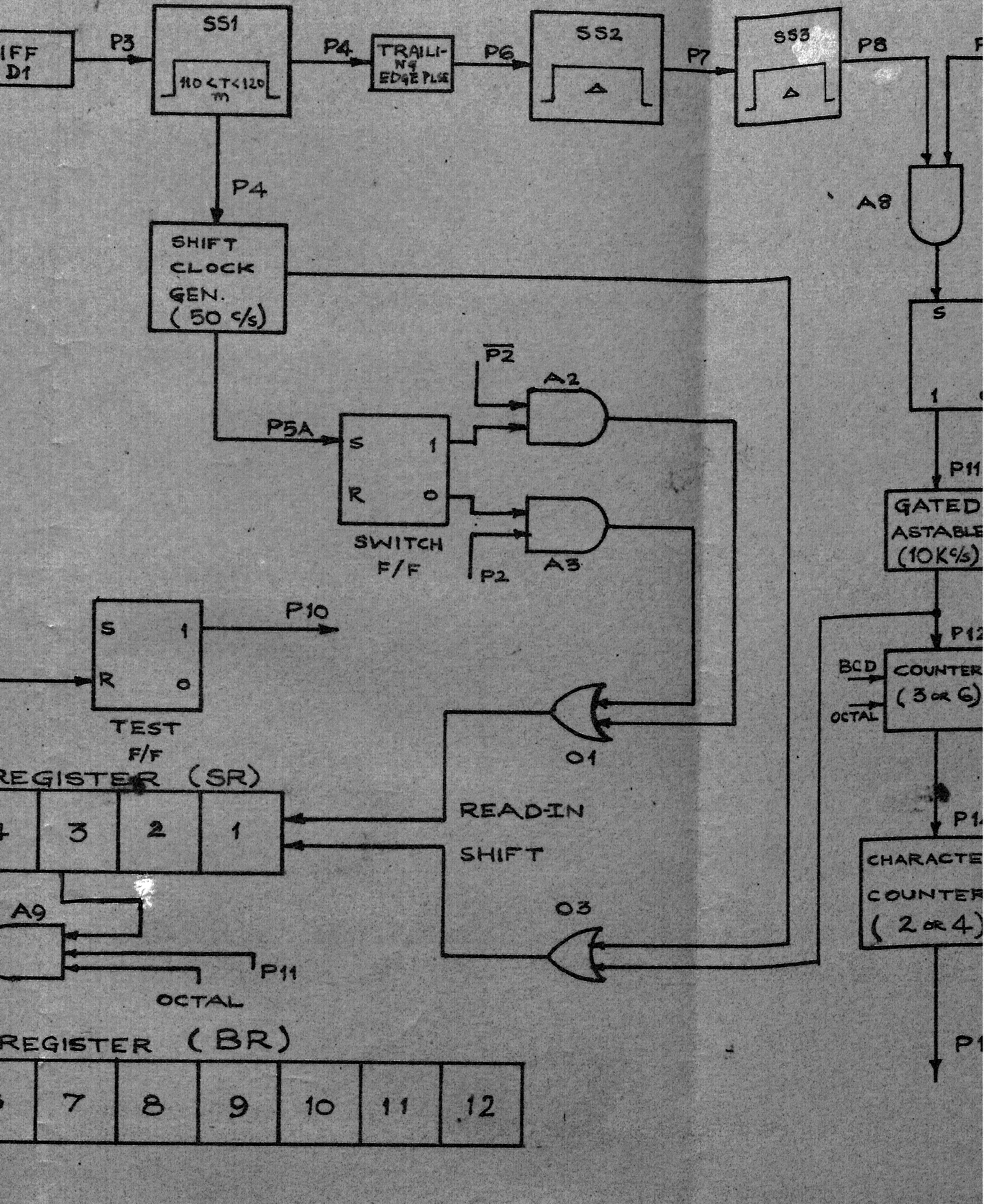
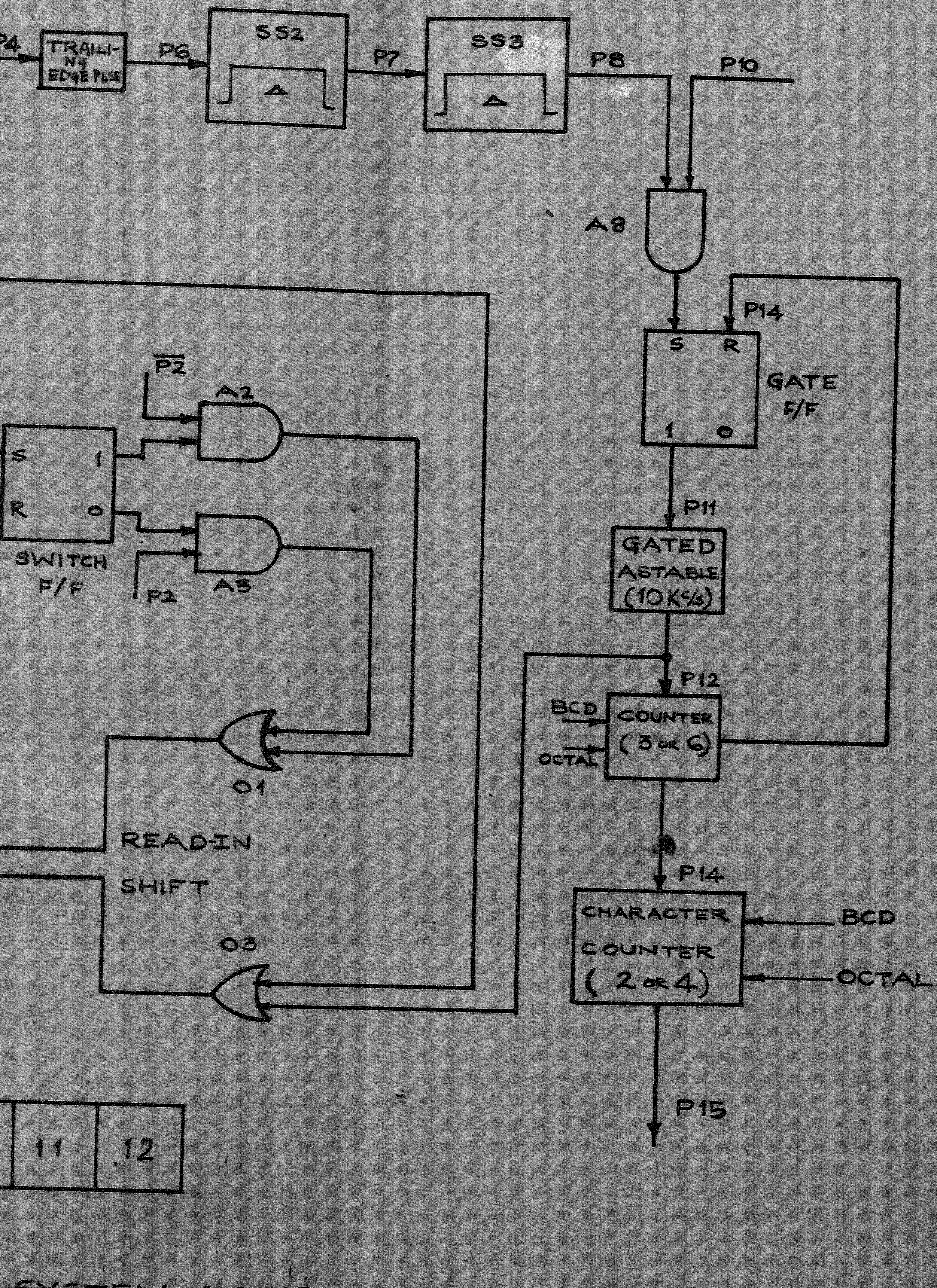


FIG 5.1A INPUT SYSTEM LOGIC



SYSTEM LOGIC

The READ cycle is now accomplished in two phases. In the first phase, information from the Teleprinter is entered into the six-bit Shift Register (indicated as SR1 through SR6 in Figure 5.1A). End of this operation is indicated by the generation of the pulse P6 at which instant processing of information in the Shift Register is carried out. In phase two of the operation, the character code in SR is shifted serially into the Input/Output Buffer Register (indicated as BR1 through BR12 in figure 5.1A). Under control from the CPU, either three or six bits are transferred depending on the mode selected (OCTAL or BCD).

We will now trace the path of information flow in the two phases with the aid of the logic diagram of figure 5.1A and its associated timing chart of figure 5.1B.

Phase I

When a key is depressed on the Key Board of the printer, the corresponding character is transmitted in the form of a series of five coded impulses alongwith START and STOP pulses to distinguish the beginning and end of each individual character. This pulse train, indicated as PO is first level adjusted to confirm to the logic levels of the electronic circuitary and passed through the gate A1 which has been enabled by a READ command from the CPU. This level-adjusted waveform is indicated as P1, P2 in the timing chart.

The first ZERO-to-ONE state transition of P2 sets a START flip flop whose output is differentiated to yield a pulse P3. This

pulse indicates the START of the character sequence with which all operations in the system have to be synchronized. P3 then triggers a single shot (SS1) whose output P4 provides the gating waveform to the shift clock generator. The delay period of SS1 has been preset to gate exactly six pulses of the astable.

The Shift Clock Generator is shown in figure 5.2. The gated astable is normally quiescent when no gating waveform is present; and is triggered on by the input to produce square wave output of pulse width 10 m sec. It stays in the astable state for a period (equal to 120 m sec) specified by the gate input. The leading negative-going edge of the output is differentiated and pulse-shaped (by passing through a single-shot) to obtain a pulse train having the following characteristics:

i. the period of the pulse train is 20 m sec
ii. there are exactly six pulses.

This waveform, P5, is the shift clock to the shift register.

The READ-IN to the Shift Register is obtained in the following manner: It was mentioned earlier that alternate pulses of the information input, P2, have to be complemented before being entered into the SR. This is accomplished by the logic using the SWITCH flip flop, gates A2, A3 and 01. This part of the input logic, with its timing diagram, is repeated in figure 5.3A and 5.3B.

The SWITCH flip flop is triggered by the Shift Clock P5; its complementary outputs P16 and P17 are then sampled alternately with P2' and P2 (the complementary input signals from the Teleprinter).

The resulting logical OR of P18 and P19 is the READ-IN to the SR. It was mentioned earlier that only the second and the fourth bits of the five-unit code should be complemented. However, in the process above, the START pulse is also complemented. This is of no consequence in the final analysis since the first bit is a SHIFT bit which in any case **is to be modified** at a later stage.

Thus the serial information from the Teleprinter has been entered into the shift register. The end of this operation is signalled by the trailing edge of the gating waveform, P4.

<u>Phase II</u>

The pulse, P6, generated at the trailing edge of the one shot output signals the end of phase I. Before transferring the information from SR into BR, the following preliminary processings have to be performed.

1. <u>Illegal character check:</u>

The following characters are used for printer control and initialization and during READ-IN need not be transmitted:

	Teleprinter Code	Computer Code A B C D E
LETTERS SHIFT	0 0 0 0 0	0 1 0 1 0
FIGURES SHIFT	0 0 1 0 0	0 1 1 1 0
CARRIAGE RETURN	1 1 1 0 1	1 0 1 1 1
LINE FEED	1 0 1 1 1	1 1 1 0 1
SPACE	1 1 0 1 1	1 0 0 0 1
UNUSED	1 1 1 1 1	1 0 1 0 1

When any of these combinations is sensed at the instant P6 appears, a

CD \ AB	00	01	11	10
00				
01		1		
11		1		
10				

$E = 0$

CD \ AB	00	01	11	10
00				1
01				
11				1
10			1	1

$E = 1$

$$T = \bar{A}BD\bar{E} + AC\bar{D}E + A\bar{B}\bar{D}E + A\bar{B}CE$$

Fig. 5.4A : KARNAUGH MAP FOR T

pulse is routed through the Illegal Character Check Matrix which resets the TEST flip flop thus indicating to the control that the character in the shift register will not be transferred to the Buffer Register.

A Karnaugh Map reduction of the truth function of these combinations is shown in figure 5.4A. From this we get,

$$T = \bar{A}BD\bar{E} + AC\bar{D}E + A\bar{B}\bar{D}E + A\bar{B}CE$$

A minimal realization using AND and OR gates is shown in figure 5.4B. This uses four 5-input AND gates and one, 4 input OR gate. The same function, realized in terms of NOR gates, is shown in figure 5.4C. Here we need four 5-input one 4-input and one 2-input NOR gates.

2. <u>Shift Signal Flagging</u>:

It was mentioned earlier that the last bit (SR 6) of the code is interpreted as the shift bit. For this purpose, the code entered in SR1 through SR5 is checked for the shift signal and correspondingly a SHIFT flip flop is set or cleared depending on the shift signal present. Pulse P7, obtained by delaying P6 slightly, is used to transfer the contents of the SHIFT flip flop into SR6. SHIFT flip flop will stay set or cleared depending on whether the last received shift signal was LETTERS or FIGURES respectively; and for every subsequent character SR6 will contain the same information as SHIFT flip flop till a shift signal to the contrary is received.

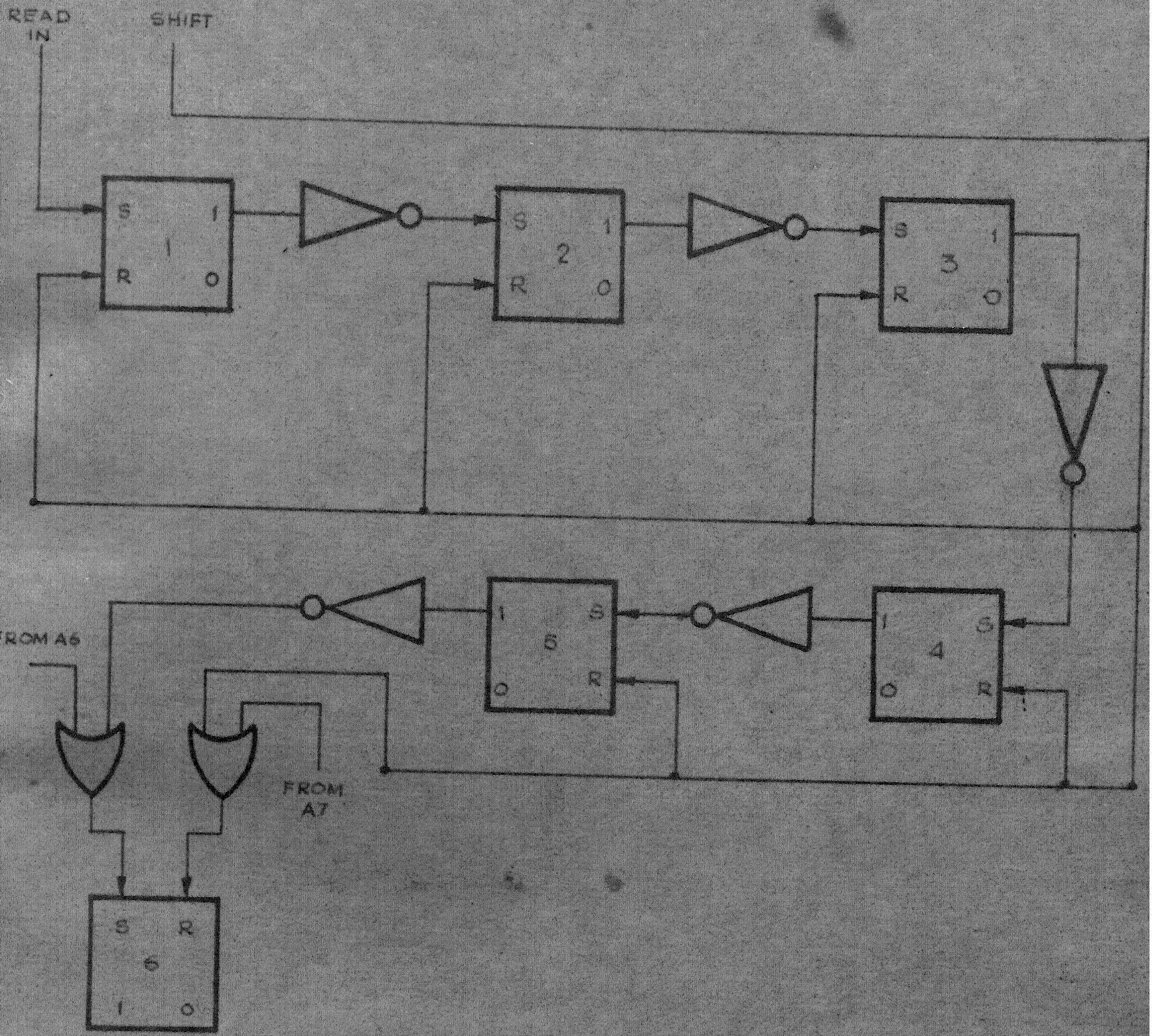


FIG. 5·5 SHIFT REGISTER CONNECTION

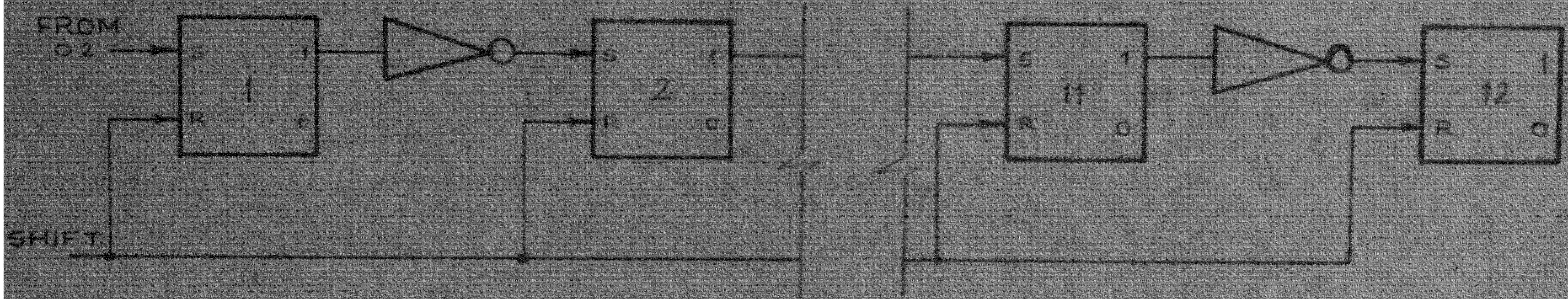


FIG 5.6 I/O BUFFER REGISTER

When these operations have been completed and the information in SR is not one of the illegal characters, then the TEST flip flop stays set which enables gate A8. The next phase of the operation is to transfer the contents of SR into BR under control from CPU depending on the mode selected (BCD or OCTAL).

In the case of BCD, gate A10 is enabled and all the six bits are transmitted to BR through A10 and 02. For OCTAL, gate A9 is enabled and only the three least significant bits are routed through to BR via gates A9 and 02. This transfer of information can be performed at an arbitrary rate; only condition being that the transfer should be completed before the end of the STOP mark of the character period. A 10 KHz gated astable was chosen for this purpose. In this case, we need either six (BCD) or three (OCTAL) pulses. The gating wave form, P11, is obtained from a flip flop which sets at the instant P8 arrives and triggers the astable ON. The astable output (after pulse-shaping as before) is then counted by a counter of three (OCTAL) or six (BCD) which clears the flip flop at the end of the prescribed count and hence turns off the astable. Thus we obtain the exact number of pulses, P12, out of the astable. This P12 is then the shift clock to both the Shift Register and the Buffer Register as shown. Depending on the mode selected, either three or six bits are transferred from SR into BR with the least significant bit from SR 1 occupying BR1 of Buffer Register.

The counter output, P14, is used to keep track of the number of characters being entered. The character counter is a two-bit counter which counts either two or four pulses depending on whether BCD or OCTAL mode is selected. When the prescribed count is finished, the counter output clears the READ flip flop which disables gate A1 and thus one cycle of READ operation is complete. Simultaneously, the OPCOMPLETE line goes down (to the logical ONE state) thus signalling to the CPU that the READ cycle is finished and the contents of the Input/Output Buffer Register can be transferred to the computer memory.

CHAPTER VI

OUTPUT FROM THE COMPUTER

In this stage, information from the Buffer Register has to be written out on the Teleprinter. The Buffer may contain either two characters (BCD) or four octal digits (OCTAL). In one cycle of WRITE operation, all the characters in the Buffer have to be printed out in a serial order starting with the most significant digit.

A complete logic of the output from the computer is illustrated in figure 6.1.

WRITE command from the CPU sets a WRITE flip flop which enables gate A1 to READ-IN information from the Buffer into the Shift Register. Simultaneously, the OPCOMPLETE line goes up (to the logical ZERO state) thus indicating to the CPU that the output unit is busy. The unit is now ready to execute one cycle of WRITE operation.

The entire process of writing out one character on the Teleprinter is accomplished in two stages.

Stage I

Information from the Buffer is first transferred into the Shift Register. This requires a shift clock which has either three or six pulses depending on the mode selected (OCTAL or BCD) from the CPU. The Shift Clock Generator consists of a gated astable whose

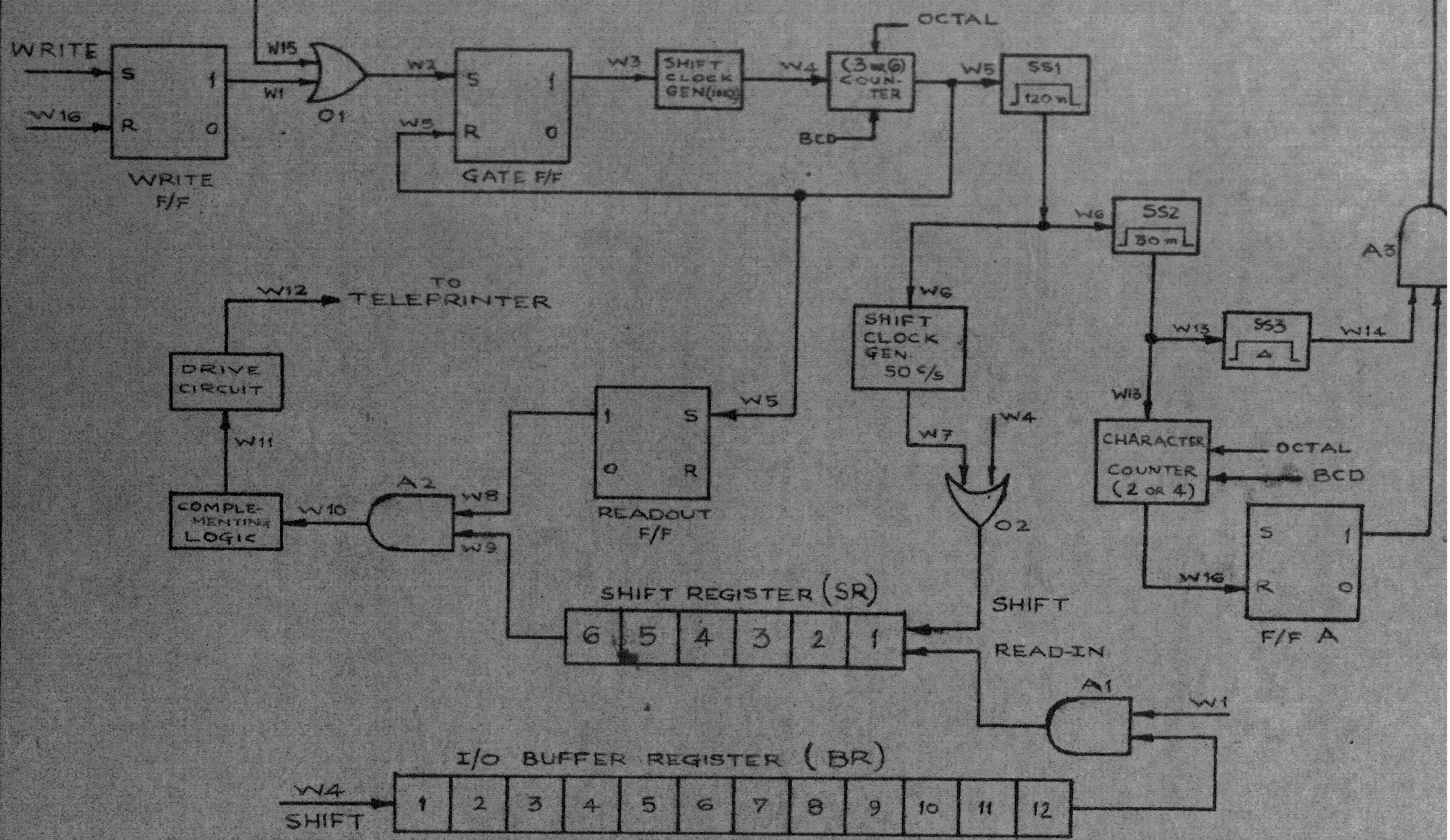


FIG 6.1 OUTPUT LOGIC DIAGRAM

square wave output is differentiated and pulse-shaped (by passing through a single shot) to obtain the shift clock. The gating waveform is obtained from the GATE flip flop which is set by the WRITE call from the CPU. The clock pulses are counted to either three or six by a counter and at the end of the prescribed count the GATE flip flop is cleared thus turning off the astable. Thus a precise number of shift pulses necessary to transmit information from BR into SR is obtained. This Shift Clock is indicated as W4 and the counter output as W5 in figure 6.1.

The information in SR is now ready to be fed into the Teleprinter. However, at this instant, following preliminary operations are carried out:

1. A READ OUT flip flop is set which enables gate A2 to transmit the information from the Shift Register into the Teleprinter.
2. Flip Flop SR6 of the Shift Register is cleared. This enables the use of SR6 to store the START pulse while the information bits are stored in SR5 through SR1. The content of SR6 is finally interpreted as a SPACE impulse when the character is being serially fed into the Teleprinter. Thus this pulse would represent the START of the character period.

Stage II

Now the character code in the Shift Register has to be fed serially into the Teleprinter. This is initiated by triggerring a single shot, SS1, whose period has been preset to gate exactly six pulses out of a Shift Clock generator. The Single Shot output provides the necessary gating to the 50 C/s gated astable whose square wave output is differentiated and pulse-shaped (by passing through a single shot) to obtain the shift clock, W7, as shown in figure 6.1.

The signal read-out of the shift register is passed through a simple logic to complement alternate pulses starting with the first pulse. This logic is discussed at length in the previous chapter on the Input to the computer. The resulting signal, which is in the proper Teleprinter Code, is applied to the Drive Circuit which provides the drive necessary to the Teleprinter Receive Electromagnet.

By the end of this transfer operation, a START impulse and five coded information impulses have been transmitted on the Teleprinter. The rest of the character period (30 m sec) is a marking impulse to represent a STOP signal. For this purpose, a single shot, SS2, of delay width 30 msec is now triggered on. The trailing edge of this single shot output, W13, indicates the end of the character period.

This marks the completion of the print out of one character. The same procedure is repeated for all the characters in the Buffer. The printing out of the second character is initiated right after the end of the first by routing the pulse W13, generated at the trailing edge of the SS2 output, back to the gate 01. Gate A3 stays enabled by the output of the flip flop A till all the characters have been printed out.

The character counter is a two-bit counter which counts to either two or four depending on the mode selected (BCD or OCTAL) under control from the CPU. At the end of the prescribed count, flip flop A resets thus disabling gate A3. Similtaneously, the WRITE flip flop is also reset. This causes the OPCOMPLETE line to go up (to the logical ZERO state) signalling to the CPU that the contents of the Input/Output Register have been printed out and the Input/Output Unit is now free. Further WRITE cycles can be initiated from the CPU by means of WRITE commands alongwith the appropriate mode selecting signal (BCD or OCTAL).

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APPENDIX

LIST OF SYMBOLS

A bar (–) over a Letter Symbol represents the maximum value of the variable; while a bar below the Symbol denotes the minimum value of the parameter.

V_{cc} = Collector Supply Voltage

$V_{CE(sat)}$ = Collector Saturation Voltage

$V_{BE(ON)}$ = Base-to-Emitter Voltage under saturation condition of the transistor

V_{γ} = Cut-in voltage

I_{CBO} = Collector-to-BaseLeakage Current (cut-off)

I_{c} = Collector Current

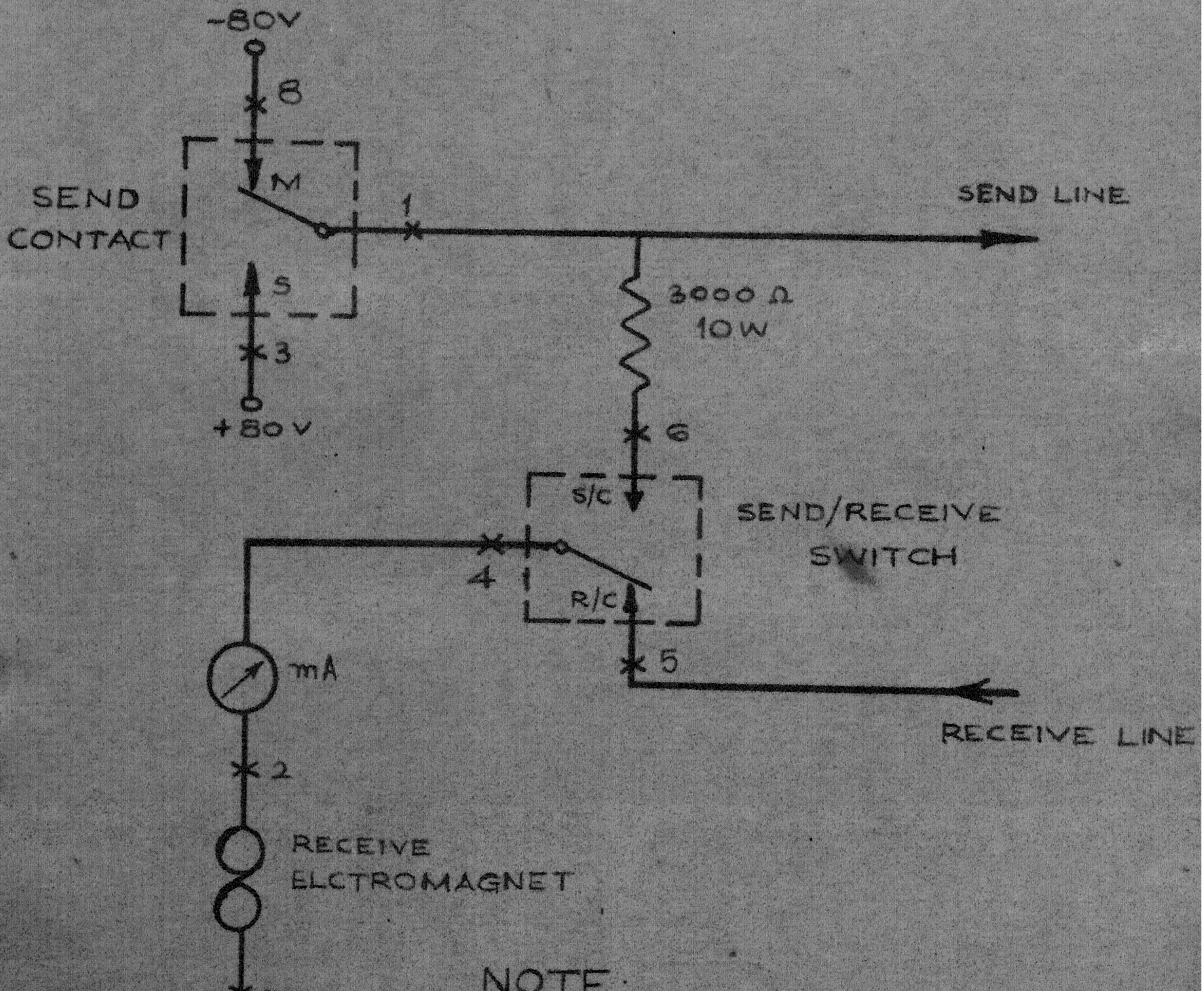
R_{c} = Collector load resistance

β_{min} = Least value of Collector-to-Base Current gain

APPENDIX A1

SCHEMATIC OF CONNECTIONS FOR THE WORKING OF HINDUSTAN TELEPRINTER MODEL (T2-CN)

(DOUBLE CURRENT SIMPLEX, ON TWO LEADS)

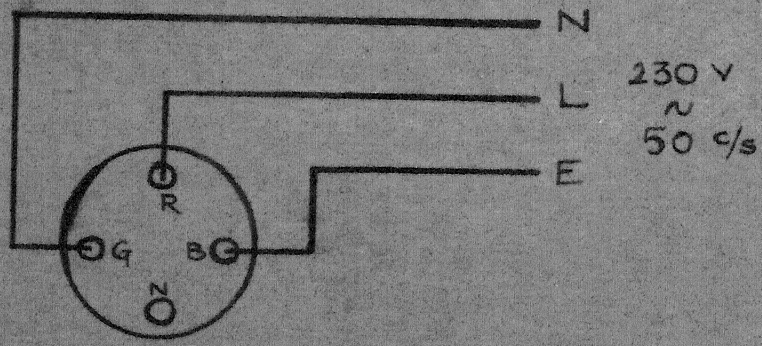


NOTE:

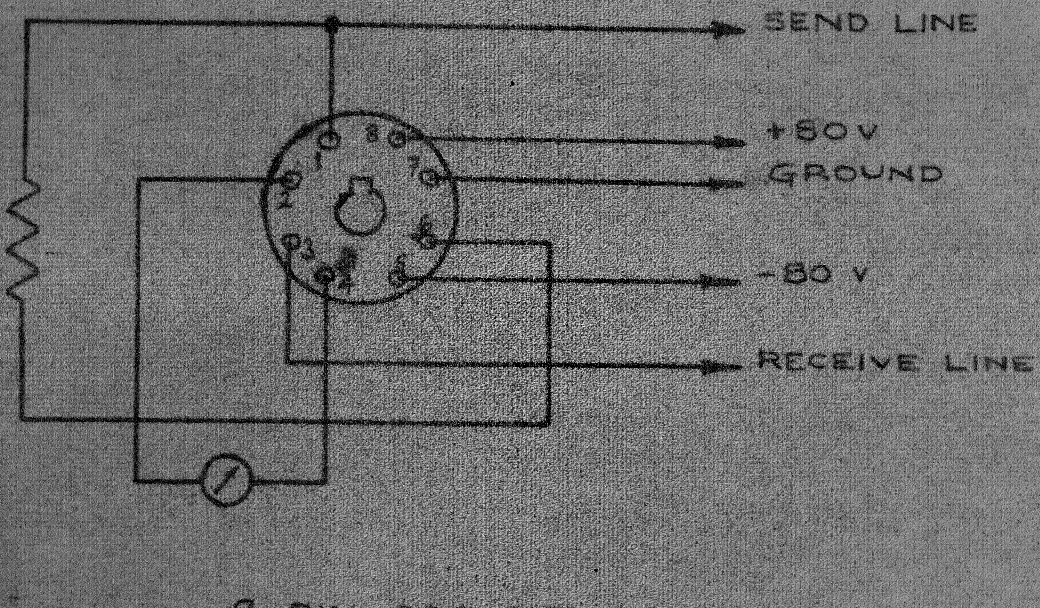
× INDICATES POINTS OF CONNECTION FROM 8-PIN PLUG TO SOCKET.

APPENDIX A2

WIRING OF SET



4-PIN SOCKET

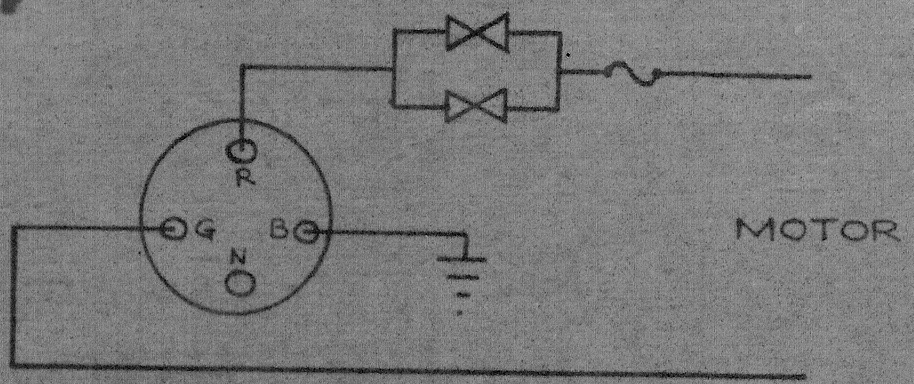


8-PIN SOCKET

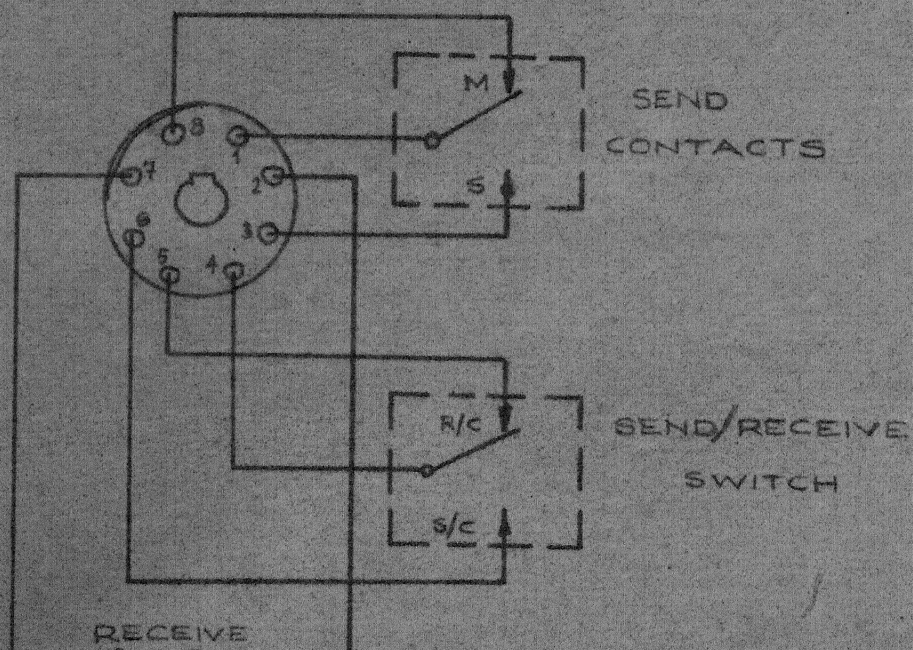
NOTE: SOCKET HOLD DESIGNATIONS ARE AS VIEWED FACING HOLES.

APPENDIX A3

INTERNAL CONNECTIONS OF TELEPRINTER



4-PIN PLUG



8-PIN PLUG

NOTE: PLUG PIN DESIGNATIONS ARE AS VIEWED FACING

APPENDIX 'B'

TELEPRINTER AND COMPUTER CODES

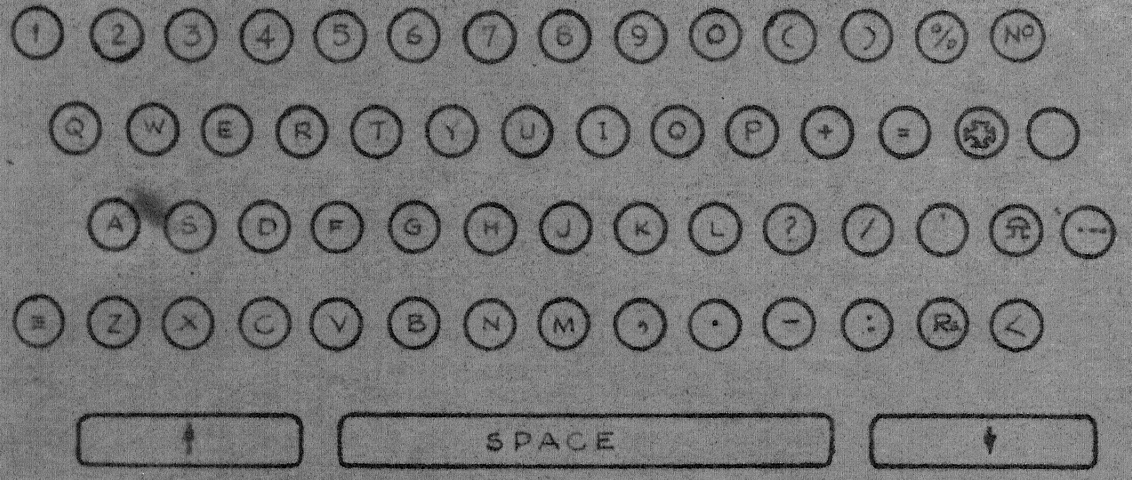
NOTE: In the case of Teleprinter codes

'0' Represents = Marking impulse
'1' represents = Spacing impulse

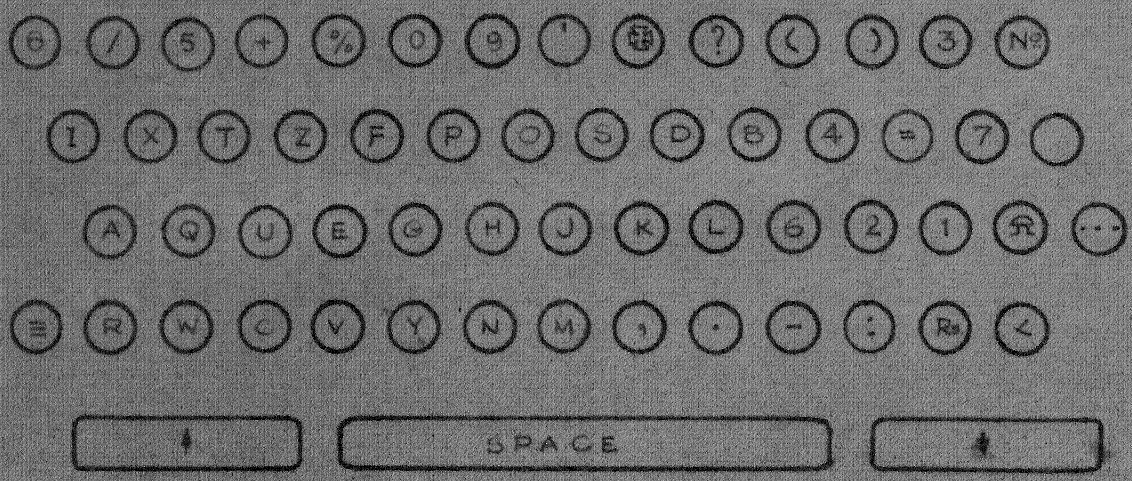
CHARACTER		STANDARD TELE-PRINTER CODE (CCITT,No.2UNIT)	TELEPRINTER CODE, AFTER MODIFICATIONS	INTERNAL COMPUTER CODE
LETTERS SHIFT	FIGURES SHIFT			
A	-	00111	00111	01101
B	?	01100	10010	11000
C	:	10001	10001	11011
D	✠	01101	11100	10110
E	3	01111	01001	00011
F	%	01001	11110	10100
G	No	10100	10100	11110
H	Rs	11010	11010	10000
I	8	10011	00010	01000
J	BELL	00101	00101	01111
K	(	00001	00001	01011
L	)	10110	10110	11100
M	.	11000	11000	10010
N	,	11001	11001	10011
Ø	9	11100	00011	01001
P	0	10010	01010	00000

Q	1	00010	01011	00001
R	4	10101	01110	00100
S	'	01011	10011	11001
T	5	11110	01111	00101
U	7	00011	01101	00111
V	=	10000	10000	11010
W	2	00110	01000	00010
X	/	01000	00110	01100
Y	6	01010	01100	00110
Z	+	01110	10101	11111
CARRIAGE RETURN (<)		11101	11101	10111
LINE FEED (≡)		10111	10111	11101
LETTERS SHIFT		00000	00000	01010
FIGURES SHIFT		00100	00100	01110
SPACE		11011	11011	10001
UNUSED COMBINATION		11111	11111	10101

APPENDIX - C2



a) ORIGINAL KEYBOARD ASSEMBLY



b) KEYBOARD ASSEMBLY AFTER MODIFICATION

APPENDIX – D

```
EG015                                         FORTRAN SOURCE LIST
   ISN          SOURCE STATEMENT

     0 £IBFTC
     1          INTEGER CODE1(26,5),CODE2(16),TEMP(26,5)
     2          DIMENSION NAME(26),NUKEY(10)
     3          COMMON NAME,TEMP,CODE2,NUKEY
     4          READ 50,(NAME(I),(CODE1(I,J),J=1,5),I=1,26)
    15     50   FORMAT(2X,1A6,5X,5I1)
    16          READ 53,(NUKEY(I),I=1,10)
    23     53   FORMAT(2X,1A6)
    24          PRINT 52
    25     52   FORMAT(1H1,20X,*CHARACTER*,10X,*CODE*/)
    26          PRINT 55,(NAME(I),(CODE1(I,J),J=1,5),I=1,26)
    37     55   FORMAT(23X,1A6,10X,5I1)
    40          DO 1 I=1,26
    41          DO 1 J=1,5
    42      1   TEMP(I,J)=CODE1(I,J)
    45          DO 6 I=1,10
    46      6   CODE2(I)=I-1
    50          CALL CALC(CODE1)
    51          DO 2 K=1,4
    52          KK=5-K
    53          DO 2 J1=1,KK
    54          DO 3 I=1,26
    55          DO 3 J=1,5
    56      3   CODE1(I,J)=TEMP(I,J)
    61          CALL INVERT(CODE1,J1)
    62          JJ=J1+K
    63          DO 2 J2=JJ,5
    64          CALL INVERT(CODE1,J2)
    65          CALL CALC(CODE1)
    66      2   CONTINUE
    72          DO 4 I=1,5
    73          DO 5 J=1,26
    74          DO 5 K=1,5
    75      5   CODE1(J,K)=TEMP(J,K)
   100          CALL INVERT(CODE1,I)
   101      4   CALL CALC(CODE1)
   103      7   CONTINUE
   104          STOP
   105          END
```

```
  ISN       SOURCE STATEMENT

    0 &IBFTC INV      NODECK
    1           SUBROUTINE INVERT(X,N)
    2           INTEGER X(26,5)
    3           DO 101 I=1,26
    4           IF(X(I,N).EQ.1)GO TO 102
    7           X(I,N)=1
   10           GO TO 101
   11   102     X(I,N)=0
   12   101     CONTINUE
   14           RETURN
   15           END
```

```
G015                                            FORTRAN SOURCE LIST
   ISN         SOURCE STATEMENT

     0 £IBFTC CALC      NODECK
     1         SUBROUTINE CALC(Y)
     2         INTEGER Y(26,5),C(16),DEC(26),SAVE(16),CODE2(16)
     3         DIMENSION NAME(26),TEMP(26,5),TEST(16),NUKEY(10)
     4         COMMON NAME,TEMP,CODE2,NUKEY
     5         N=0
     6         DO 201 I=1,26
     7         DO 202 J=1,5
    10   202   C(J)=Y(I,J)
    12         DO 203 J=2,5
    13   203   C(1)=2*C(1)+C(J)
    15         DEC(I)=C(1)
    16         DO 201 J=1,10
    17         IF(DEC(I).NE.CODE2(J))GO TO 201
    22         N=N+1
    23         SAVE(J)=I
    24   201   CONTINUE
    27         IF(N.NE.10)RETURN
    32         PRINT 54
    33    54   FORMAT(1H1,20X,*TELEPRINTER CODE*,5X,*ORIGINAL KEY*,5X,
              1*NEW KEY*/)
    34         DO 206 M=1,10
    35         N=SAVE(M)
    36   206   PRINT 51,(TEMP(N,J),J=1,5),NAME(N),NUKEY(M)
    44    51   FORMAT(26X,5I1,15X,1A6,8X,1A6/)
    45         RETURN
    46         END
```

CHARACTER	CODE
A/-	00111
B/?	01100
C/:	10001
D/$	01101
E/3	01111
F/%	01001
G/NO.	10100
H/RS.	11010
I/8	10011
J/BELL	00101
K/(	00001
L/)	10110
M/.	11000
N/,	11001
O/9	11100
P/0	10010
Q/1	00010
R/4	10101
S/'	01011
T/5	11110
U/7	00011
V/=	10000
W/2	00110
X//	01000
Y/6	01010
Z/+	01110

TELEPRINTER CODE	ORIGINAL KEY	NEW KEY
01110	Z/+	P/0
01111	E/3	Q/1
01100	B/?	W/2
01101	D/✠	E/3
01010	Y/6	R/4
01011	S/'	T/5
01000	X//	Y/6
01001	F/%	U/7
00110	W/2	I/8
00111	A/-	O/9

SET 1: BITS 2,3,4 COMPLEMENTED

TELEPRINTER CODE	ORIGINAL KEY	NEW KEY
01111	E/3	P/0
01110	Z/+	Q/1
01101	D/✠	W/2
01100	B/?	E/3
01011	S/'	R/4
01010	Y/6	T/5
01001	F/%	Y/6
01000	X//	U/7
00111	A/-	I/8
00110	W/2	O/9

SET 2: BITS 2,3,4,5 COMPLEMENTED

TELEPRINTER CODE	ORIGINAL KEY	NEW KEY
01010	Y/6	P/0
01011	S/!	Q/1
01000	X//	W/2
01001	F/%	E/3
01110	Z/+	R/4
01111	E/3	T/5
01100	B/?	Y/6
01101	D/✠	U/7
00010	Q/1	I/8
00011	U/7	O/9

SET 3: BITS 2,4 COMPLEMENTED

TELEPRINTER CODE	ORIGINAL KEY	NEW KEY
01011	S/'	P/0
01010	Y/6	Q/1
01001	F/%	W/2
01000	X//	E/3
01111	E/3	R/4
01110	Z/+	T/5
01101	D/✠	Y/6
01100	B/?	U/7
00011	U/7	I/8
00010	Q/1	O/9

SET 4 : BITS 2,4,5 COMPLEMENTED

APPENDIX 'E'

CIRCUIT DETAILS

E.1 Gated Astable

The circuit of the gated astable is shown in figure E.1.1.

It is a normal astable circuit which has been forced to start (or stop) oscillating at definite times by the addition of a transistor T3 in series with the emitter of T1. When the gate input to T3 is such that T3 is OFF, then T1 is OFF and T2 is ON; and the circuit is quiescent (not oscillating). When the gate input drives T3 into saturation, T1 goes ON and due to regenerative feedback T2 goes OFF. The circuit now oscillates like a normal astable till the gate input turns T3 OFF and the circuit returns to the quiescent state.

The two diodes and the two resistors have been added to give collector waveforms with vertical edges. If T1 is driven OFF, its collector falls immediately to $-V_{cc}$ so that D1 is reverse-biased and T2 goes into saturation. The saturation base current of T2 passes through C and R_1 rather than through R_c. Hence the collector output waveform has vertifical edges.

Timing considerations

The timing resistor, R, is chosen to ensure saturation of the conducting transistor.

$$\bar{R} = \beta_{min} \frac{\underline{V}_{cc} - \bar{V}_{BE(ON)}}{\bar{V}_{cc} - \underline{V}_{CE(Sat)}} \underline{R}_c \qquad (E.1)$$

The period, T_{OFF}, for which either transistor is cut off (in the case of symmetrical square wave output) is given by:

$$T_{OFF} = RC \ \ln \frac{2V_{cc} + I_{CBO} R - V_{CE(Sat)} - V_{BE(ON)} - I_{CBO}R_C}{V_{cc} + I_{CBO}R - V_{\gamma}} \tag{E.2}$$

where the symbols are explained before. In the present case, using 2N995 (pnp) transistors and

$$V_{cc} = -6V$$
$$R_C = 1.5K\Omega$$
$$I_{CBO} = 1 \mu A$$
$$V_{CE(sat)} = -0.2V$$
$$V_{BE(ON)} = -0.95V$$
$$\beta_{min} = 20$$
$$V_{\gamma} = -0.5V$$

Using (E.1),

$$\bar{R} = 20 \times \frac{-5.5}{-5.6} \times 0.950 \ K\Omega$$
$$= 18.65 \ K\Omega$$

In terms of standard components,

$$\bar{R} = 15 \ K\Omega \tag{E.3}$$

Using (E.2),

$$T_{OFF} = RC \ \ln \frac{-10.664}{-5.515}$$
$$= 0.664 \ RC \tag{E.4}$$

Using relations (E.3) and (E.4) we can adjust R and C for desired periods.

E.1.1 50 C/S Astable

Here

$$T_{OFF} = 10 \text{ m sec}$$

Choosing $R = 7.5\ K\Omega$ to ensure saturation

$$C = 2.0\ \mu F$$

The circuit used is shown in figure E.1.3. The 3.3K potentiometer is used to adjust the period accurately.

E.1.2 10 K C/S Astable

Here

$$T_{OFF} = 50\ \mu\text{sec}$$

Choosing

$$R = 15\ K\Omega$$

$$C = 0.005\ \mu F$$

The circuit is shown in figure E.1.4.

E.2 Teleprinter Drive Circuit

The circuit is illustrated in figure E.2. The Teleprinter Receive Electromagnet requires 20 - 60 mA drive through a parallel combination of two coils, 240 impedance each.

The first stage helps to adjust the levels of the incoming signal to proper values so that bidirectional signal input is available at the common base lead of the complementary pair. During a positive transition, T1 provides the drive through the coils thus accounting for a SPACE signal; and T2 provides the drive during a negative input

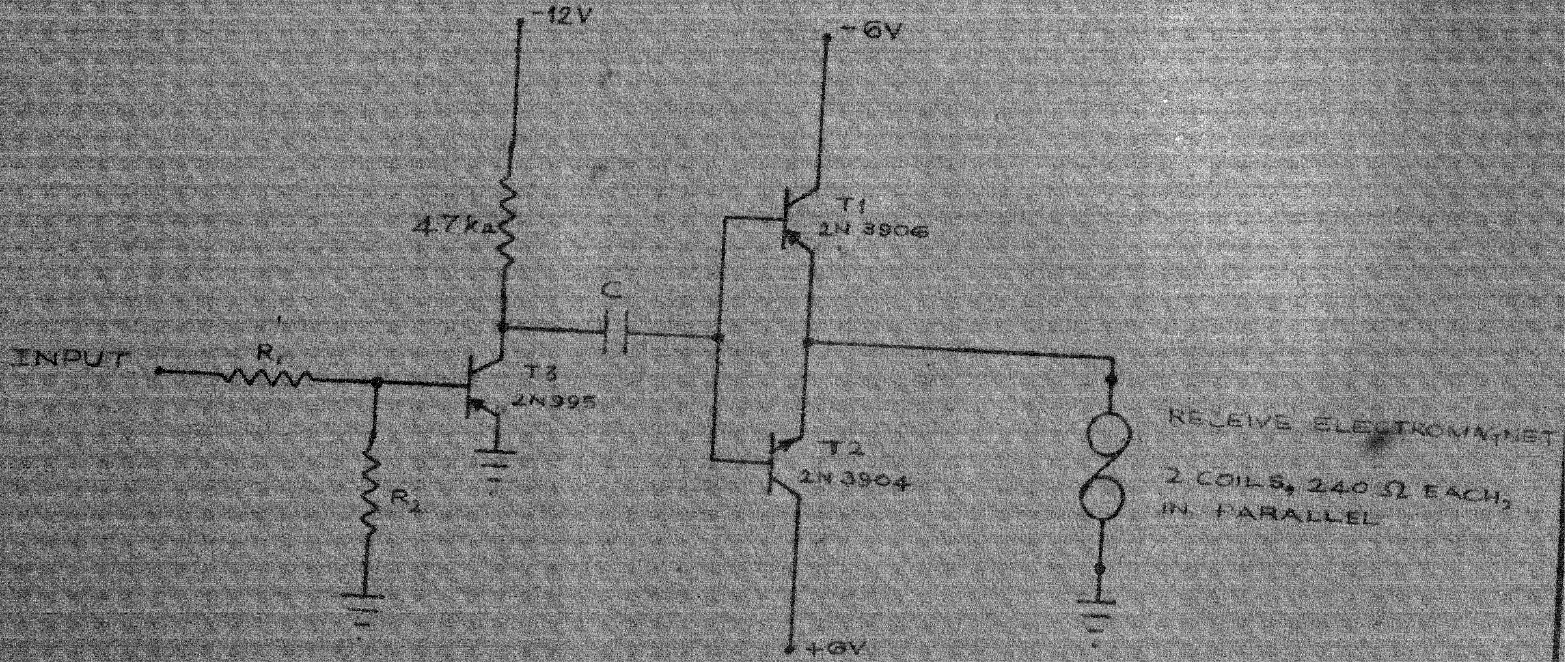


FIG E.2 : TELEPRINTER DRIVE CIRCUIT

transition thus accounting for a MARK signal. Complementary pair of transistors, 2N3904 (npn) and 2N3906 (pnp) ensure symmetrical bidirectional output.

E.3 Other Circuits

The following are the basic modules used in the system.

1. Flip flops
2. Single shots
3. Invertors
4. NOR-gates

The circuits are illustrated in figures E3A through E.3D. Details of the circuit design are given in Reference. 2.

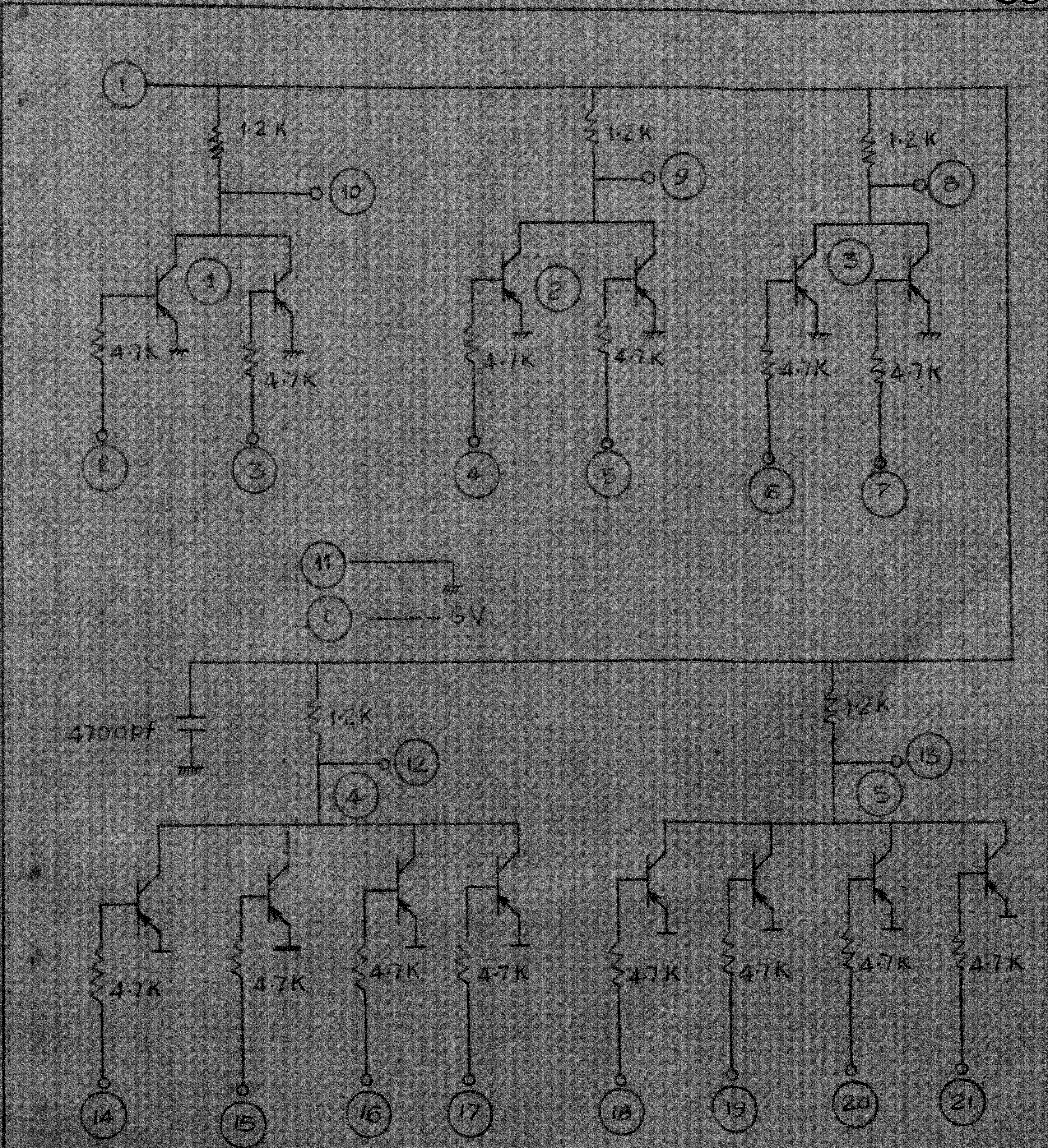
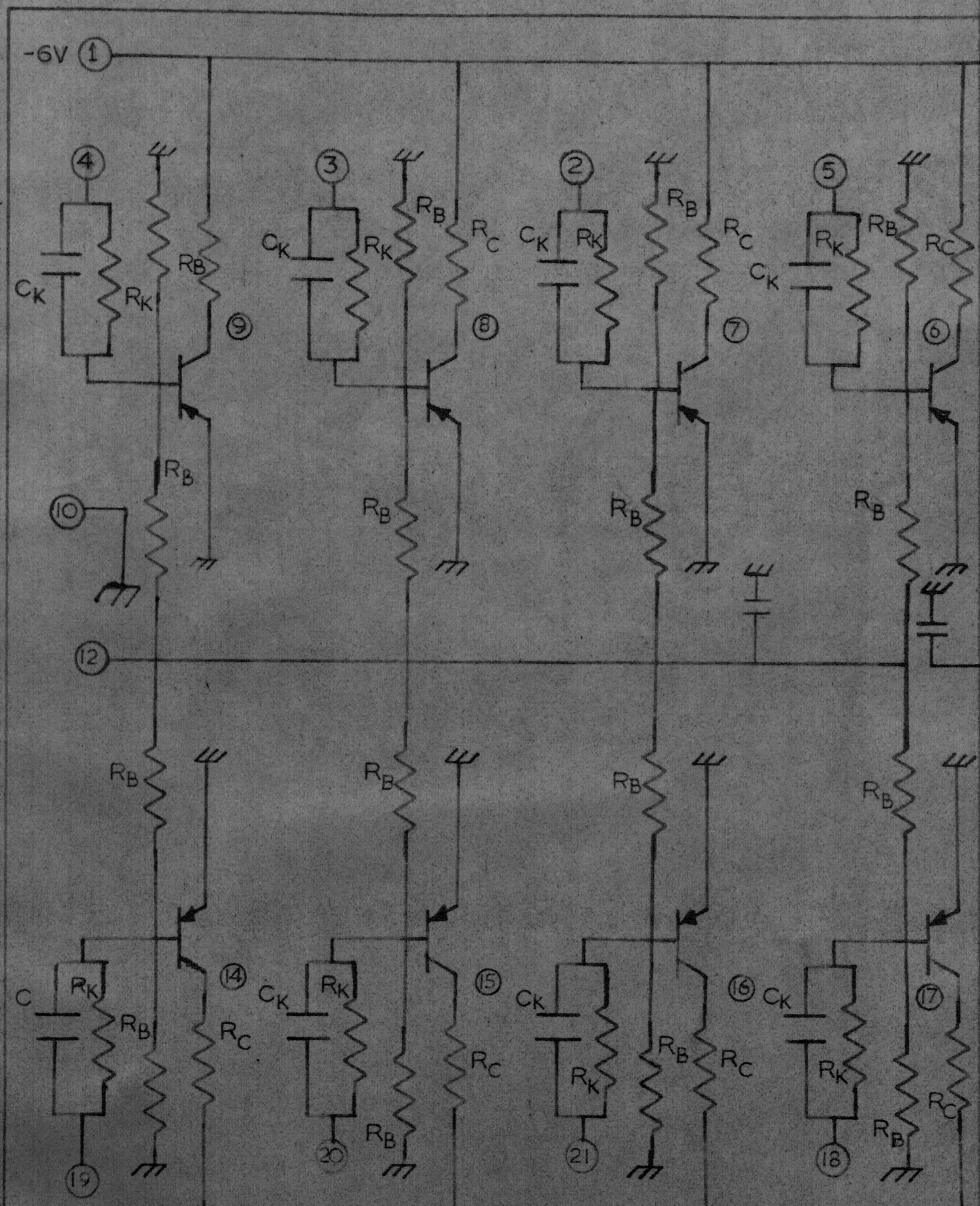
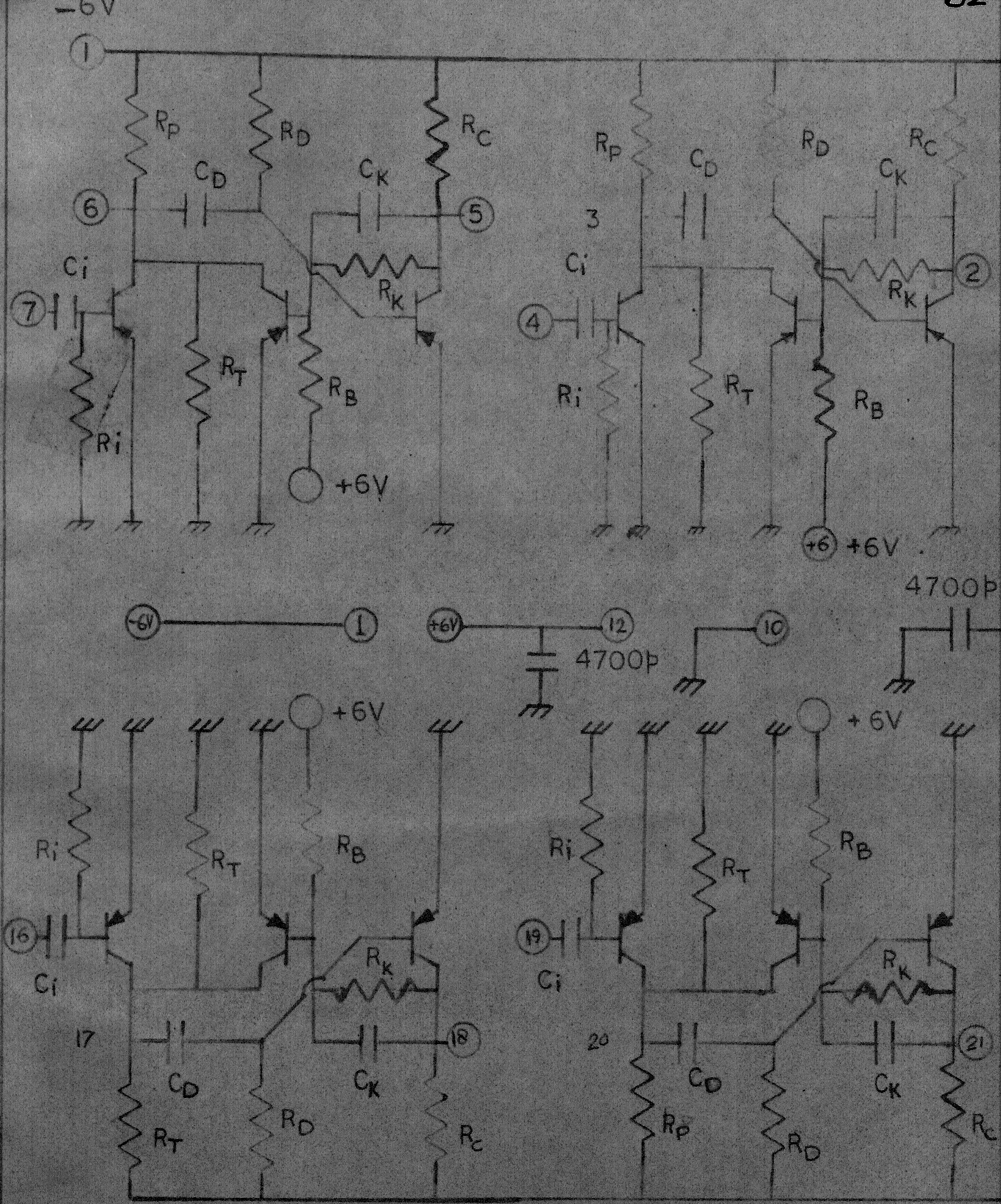


FIG. E3. B CIRCUIT DIAGRAM T.R.L. CARD



$C_K = 56pf$ $R_K = 4.7K$ $R_C = 820\Omega$ $R_B = 75K\Omega$

FIG. E3C INVERTER CARD CIRCUIT.



$R_C = 820\,\Omega$ $R_P = 750\,\Omega$ $R_T = 1K$, $R_K = 4.7K$, $R_B = 75K$, $R_D = 15K$, $C_K = 56p$, C_i 470

FIG. E.3D CIRCUIT DIAGRAM ONE SHOT CARD